

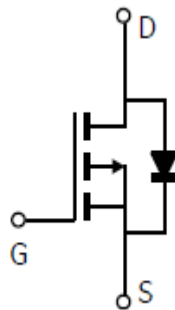
Features

- $V_{DS}=-30V/V_{GS}=\pm 20V/I_D=-30A$
 $R_{DS(ON)}=11m\Omega(Typ)@V_{GS}=-10V$
 $R_{DS(ON)}=15.5m\Omega(Typ)@V_{GS}=-4.5V$
- Low Dense Cell Design
- Reliable and Rugged
- Advanced trench process technology

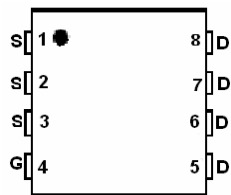
Applications

- Synchronous Rectification
- Power Management in Inverter System

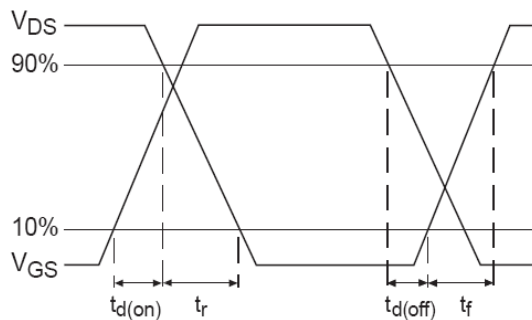
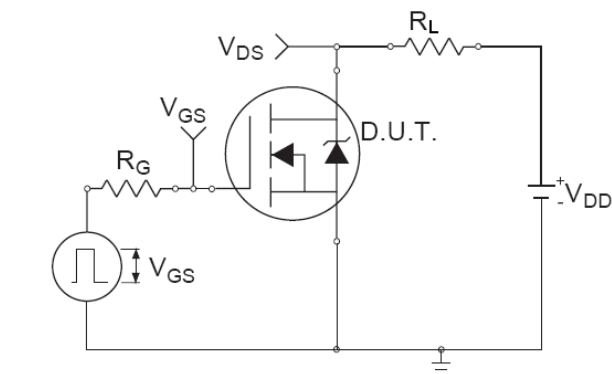
Pin Description



Marking and pin Assignment



Marking and pin assignment



Package Marking and Ordering Information

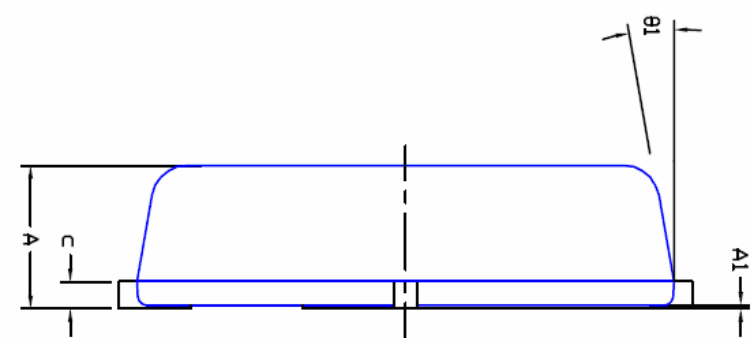
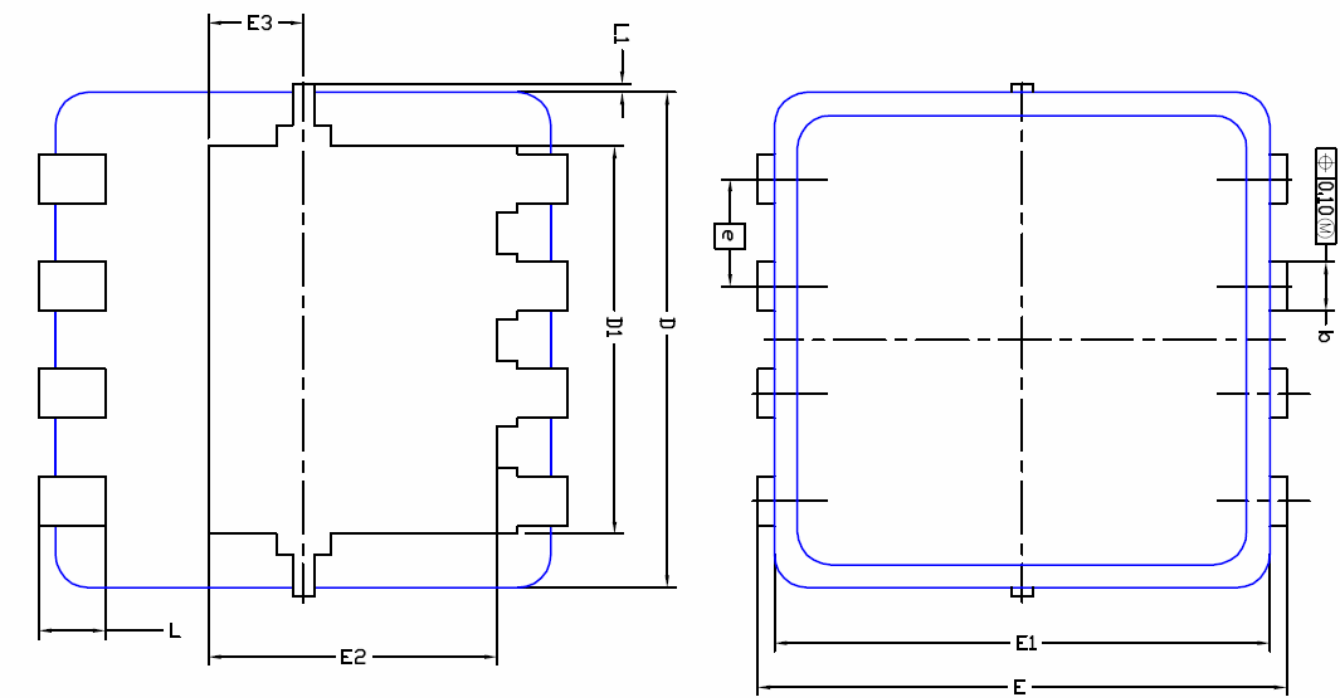
Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM30P03Q	HM30P03Q	DFN3X3-8L	-	-	-

Electrical Characteristics of CP Test (TA=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V			1	uA
		T _J =85°C			30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.6	-2.4	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =-10V, I _D =-30A		11	16	mΩ
		V _{GS} =-4.5V, I _D =-21A		15.5	20	
V _{SD}	Diode Forward Voltage	I _{SD} =-8A, V _{GS} =0V			-1.3	V
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Frequency=1MHz		6		Ω

Note: 1: Pulse test ; pulse width ≤ 300ns, duty cycle ≤ 2%.

2: Guaranteed by design, not subject to production testing.



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°